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Advancement in Ion Implantation Annealing from Seconds to Milliseconds

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Thermal processes are some of the key steps in semiconductor manufacturing. A critical issue associated with the continuous reduction of dimensions of CMOS transistors is the realization of highly conductive, ultra-shallow junctions for source/drain extensions. The temperature-time cycle has changed radically over the past 10 years. Halogen lamp-based thermal annealing, for a period of seconds, evolved to spike anneals of one second and then to flash-lamp annealing or laser annealing. These provide an ultra-sharp temperature peak of the order of milli-seconds and are favored for this kind of activation anneals. Other processes that have historically been thermally driven such as oxidation of silicon have migrated to process solutions using other drivers such as plasma activation. This contribution reviews various annealing equipment types and their annealing schemes (temperature-time cycles and gaseous ambient) and investigates the formation of ultra-shallow, highly-electrically-activated and custom-shaped junctions by discussing various annealing strategies like e.g. combinations of milli-second and halogen-lamp based rapid thermal annealing. Furthermore activities like the “re-invention” of solid phase epitaxy is discussed including the thermal stability of these junctions. Moreover, annealing of defects is always linked to the activation anneal. Therefore the deactivation of highly-activated junctions will also be shortly reviewed. Finally for Silicon the co-implantation of carbon and fluorine to reduce the dopant junction depth is noted exemplarily and some latest advancements in predictive simulation of leading edge junctions are shortly summarized.